Random Access Memory using Perovskite Materials

Oluchi N. Onwuvuche

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Intern Affiliation: Electrical Engineering, University of the District of Columbia (UDC)

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PARADIM REU Principal Investigator: Dr. Darrell Schlom, Director, PARADIM

PARADIM REU Mentor: Matthew Barone, Sirui Tan, Materials Science and Engineering, Cornell University; Mehmet Ozdogan, Mechanical Engineering, Binghamton University; Kwame Amponsah, Xallent LLC

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Contact: oluchionwuvuche@outlook.com, schlom@cornell.edu, mattbarone@me.com, st924@cornell.edu, mozdoga1@binghamton.edu, kwame.amponsah@xallent.com

Website: http://cnf.cornell.edu/education/reu/2019

Abstract:

Project was centered on creating Resistive Random Access Memory (RRAM) utilizing perovskite materials. Units of this memory device comprised of memristors whose geometry are similar to a capacitor. Lanthanum aluminate and strontium titanate ($LaAlO_3/SrTiO_3$ or LAO/STO), known for their conducting interfaces, are two perovskite materials used as the dielectric layer. Simplified chips were microfabricated to study the electrical properties of this new device. The I_{ON}/I_{OFF} ratio of the device was 68.

Background:

Low-powered resistive random access memory (RRAM) constructed out of strongly correlated materials are poised to solve decade's old problems in computing. Currently, most operating systems that utilize Von Neumann computing architectures suffer from the Von Neumann bottleneck where the constant data flow between the central processing unit (CPU) and memory presents a significant cost in power and wire delays [1]. To meet the requirements of "big data" and Internet of Things, alternative computing architectures such as *in-memory* computing has attracted much attention. Instead of moving data to and from the CPU, distributing the computation in memory can reduce latency and energy from unnecessary data fetch calls [2].

Recent developments in RRAM technologies based on strongly correlated materials which offer low power, high speed operation, and ultrahigh level integration may address the Von Neumann bottleneck by ushering in a more efficient in-memory computing. This project focused on exploring the use of $LaAlO_3/SrTiO_3$ as a key switching material in RRAM.

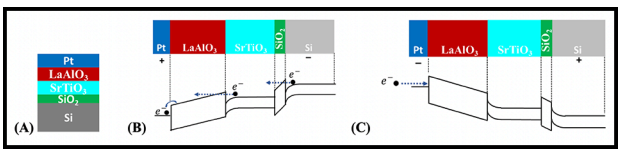

Figure 1: (A) Cross section schematic of the RRAM device. (B) Band diagram showing the low resistive state of the RRAM. (C) Band diagram depicting the high resistive state of the RRAM.

Theory:

Our RRAM device could be modeled after a capacitor as illustrated in Figure 1A and its working principle could be better understood from its band diagram shown in Figure 1B and 1C. The low resistive state (ON state) occurs when a positive voltage is applied to the top platinum (Pt) electrode and the silicon substrate is grounded (Figure 1B). The high electric field causes the electrons in the silicon substrate to tunnel across the SiO_2 layer. These electrons then again tunnel into the $LaAlO_3$ bandgap and make their way down to the Pt layer. During the transport of electrons from the silicon to the Pt layer, some of the electrons could be trapped in the $SiO_2/SrTiO_3/LaAlO_3$ layers.

Conversely, when a negative voltage is applied to the Pt layer (Figure 1C), due to the wide bandgap in the $LaAlO_3$ layer, few electrons from Pt have the energy to reach the $LaAlO_3$ conduction band. Thus the device acts like a rectifier allowing current to flow when a positive voltage is applied and blocking current flow with

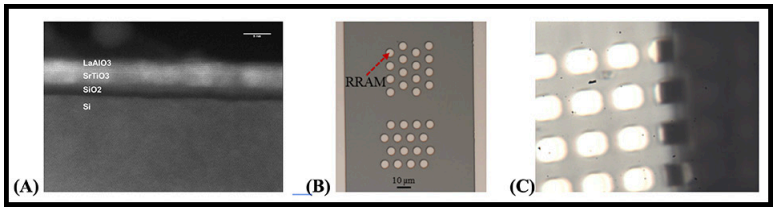

Figure 2: (A) High angle annular dark-field STEM of $LaAlO_3/SrTiO_3/SiO_2/Si$ wafer showing the existence of SiO_2 layer at the $SrTiO_3/Si$ interface. (B) Optical image of 5 μm diameter RRAM devices fabricated at the Cornell NanoScale Facility. (C) Xallent's 10 μm pitch 4-point probe lands on the Pt layer of each RRAM and current-voltage measurements are taken.

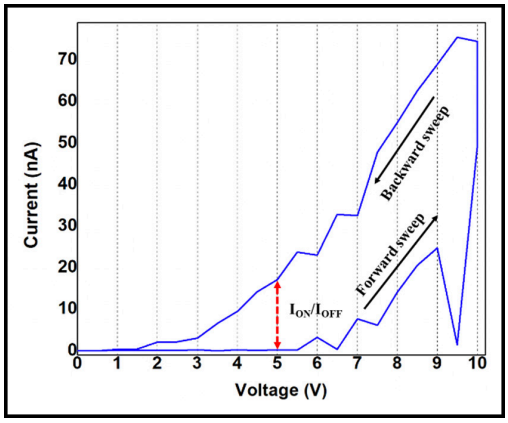

Figure 3: Current-voltage (IV) response of 16 RRAM devices. IV plot shows the electrical response of a device.

negative applied voltage to the Pt layer. The device is in the high resistive state (OFF state) when a negative voltage is applied to the Pt layer.

Fabrication:

Molecular-beam epitaxy (MBE) was used to grow $LaAlO_3/SrTiO_3$ on a silicon substrate. Five unit cells of $SrTiO_3$ followed by another five unit cells of $LaAlO_3$ were grown. When growing the sample, we filled the chamber with oxygen to enable the creation of lanthanum aluminate ($LaAlO_3$) and strontium titanate ($SrTiO_3$) from the pure metal precursors. The byproduct of this growth technique was the creation of an amorphous silicon dioxide layer (α-SiO_2) sandwiched between the silicon substrate and $SrTiO_3$. The thickness of the α-SiO_2 was 2.2 nm as shown in high angle annular dark-field STEM of Figure 2A. Thereafter, standard microfabrication techniques were used to pattern platinum electrodes on top of the $LaAlO_3$ as shown in Figure 2B.

Results:

We measured the current-voltage (IV) response of 16 RRAM devices and IV plot below shows the electrical response of a device. Xallent LLC's 10 μm pitch 4-point probe was used to make contact to the RRAM devices as shown in Figure 2C. We performed a dual continuous sweep from 0 to +10 V then back to 0 V. In the forward sweep, we observe tunneling at voltages above 5.5 V and the current reached a value of 50 nA at 10 V.

On the backward sweep, we observe a hysteresis and current gradually fells to 0.3 nA at 1 V. We predict during the forward sweep, the tunneling of the electrons caused the current to exponentially rise as well as some of the electrons could be trapped in the $SiO_2/SrTiO_3/LaAlO_3$ stack.

The observed hysteresis effect in the backward sweep could be due to trapped electrons being ejected back to the silicon substrate. This device exhibited an I_{ON}/I_{OFF} ratio of 68 at 5 V and has the potential to be utilized as a RRAM for in-memory computation.

Next Steps:

Further work on this project involves testing retention and endurance of the device (i.e. lifetime of "on" state and number of cycles until failure).

Acknowledgements:

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References:

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[2] J. Zhou, "Switching Memory and Reconfigurable Devices," Ph. D. dissertation, Department Electrical Engineering, University of Michigan, Ann Arbor, MI, 2016.