Examining Microwave Annealer for Dopant Activation in Silicon Chip in Simulation

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Abstract:
Microwave annealer have been proven to be effective to anneal Si wafer and activate the dopants at 2.45 GHz. By using COMSOL multi-physics finite-element simulator, a design of microwave waveguide connecting the microwave source to a 1cm x 1cm high resistance Si chip was made. The goal of the simulation is to see with if the waveguide design is able to distribute microwave evenly in the Si chip under different conditions added into the environment.

Introduction:
Traditionally rapid thermal annealing has been the method used to activate dopants in semiconductors. However, the heating process of rapid thermal annealing could deactivate dopants within the semiconductor, producing undesirable result. Recently, it has been proven in previous work microwave annealing was found to achieve a more efficient and stable dopant activation than rapid thermal annealing. [1] In order to anneal a silicon chip (1 cm x 1 cm) as evenly as possible, a silicon waveguide was designed previously to achieve this. [2][3] Uniformity is determined by the thermal and electrical field distribution across the surface of the 1 cm x 1cm Si chip in simulation.

Methods:
Using COMSOL multi-physics finite-element simulator. The previously made design is examined by setting electrical and thermal boundary conditions. A 1 cm x 1 cm high-resistance ($\rho = 10^5$ Ω-cm) is added on the end of the waveguide, including 3 possible interactions between Si chip, Si waveguide and the air gap between them as shown in Fig. 1. The microwave source is then added into the simulation to anneal the Si chip. As previously mentioned, the performance of the waveguide will be determined by the uniformity of thermal and electrical field distribution on top of the Si chip, measured within COMSOL using its built-in function to obtained the % deviation of field. Since the edge of the 1 cm x 1 cm Si chip tends to have an edge effect that makes the field extremely uneven near the edge, shown in Fig. 2, it is excluded by cutting the edge and using only the center 0.8 cm x 0.8 cm area, which is represented as only using the center 0.8 cm x 0.8 cm area of data when measuring the uniformity.

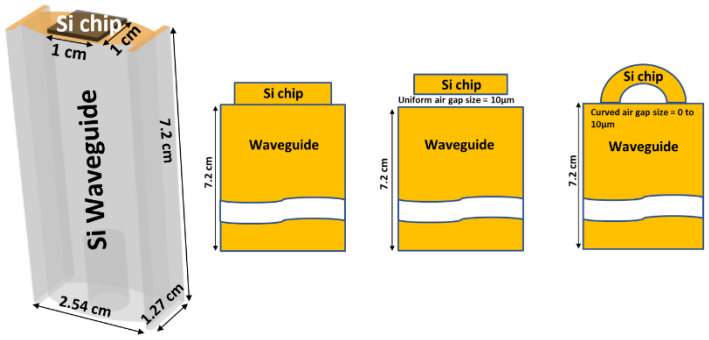

Figure 1. (Left) The set-up of the simulation with the waveguide connecting a 1 cm x 1 cm silicon chip with the waveguide and (Right three) the three cases of interactions between Si chip and waveguide previously designed. From left to right in order is: No air gap between Si chip and waveguide, a uniform air gap of 10 μm in between Si chip and waveguide, a curved air gap of size from 0 to 10 μm in between Si chip and waveguide

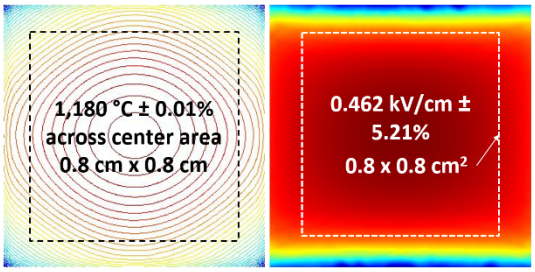

Figure 2. (Left) The temperature profile of the 1 cm x 1 cm silicon chip with a uniform air gap of 10 μm in between Si chip and waveguide
(Right) The electric field profile of the 1 cm x 1 cm silicon chip with a uniform air gap of 10 μm in between Si chip and waveguide

Result:

Using COMSOL and the setup described in Fig. 1, the electric field and temperature profile can be extracted for all three cases described above. It was founded that within air gap size of 10 μm, the difference between the three cases is small and uniform air gap will serve as a good representation of the rest. As shown in Fig. 2, both electric field and temperature are unform and has small deviation across the chips surface, which is desirable. The variation of electric field was less than 6% across the center 0.8 cm x o.8 cm area, while the variation of temperature was less than 0.1% in the same area. Even when adding an thin 30 nm epitaxial layer of high conductivity (ρ = 1 mΩ-cm) Si on the top of the Si chip, the variation of electrical field remain less than 7%.

Conclusion and Future Works:

From the result section it is shown the waveguide design was promising. As we now know the waveguide design is valid to take on different alteration in the simulation while being able to maintain a uniform microwave effect on the Si chip. As all of the previous work done in this report was in simulation, the next step will be creating a physical prototype and conduct physical experiments to take measurements.

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[3] J. C. M. Hwang, M. Javad Asadi, G. Fabi, and C. P. Savant, "Microwave annealer for semiconductor wafers," U.S. Patent Application No. 63/341,129, May 12, 2022.