3D Imaging at the Atomic Scale

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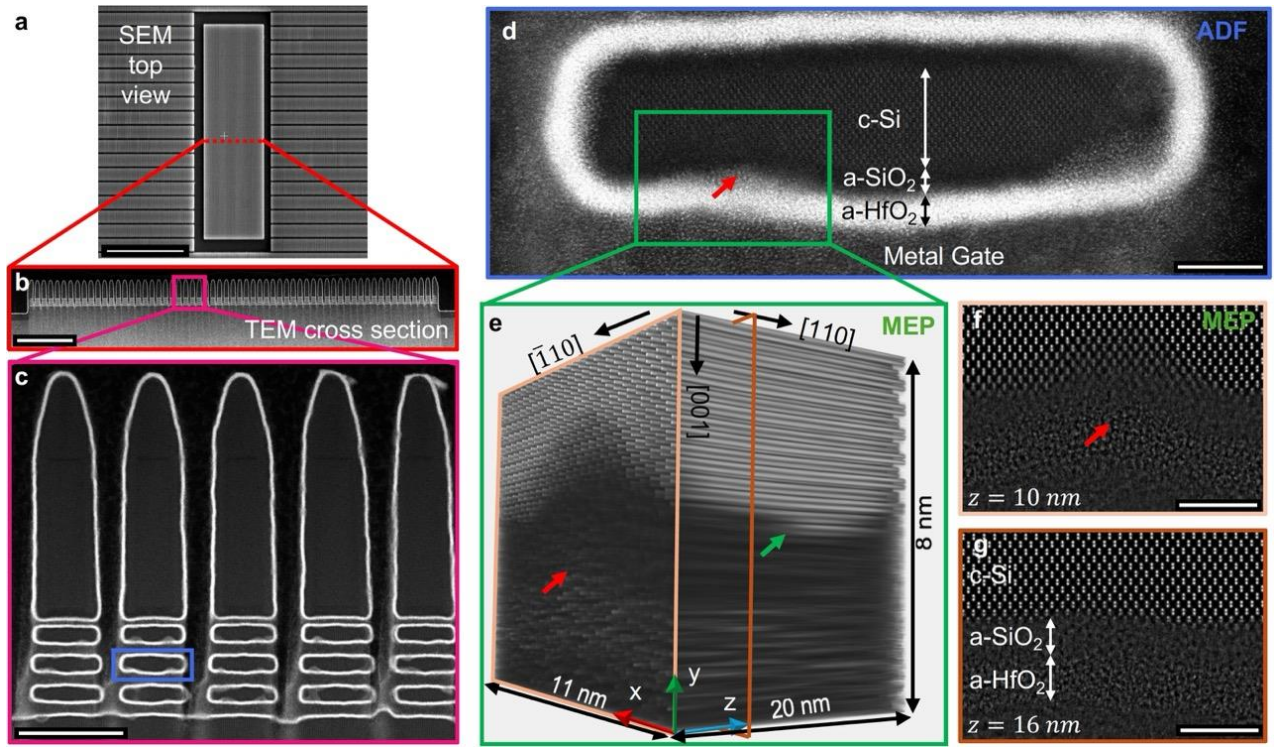
Next-generation semiconductor devices are adopting feature sizes of just a few nanometers, with individual components about a dozen atoms wide. The characterization of such tiny structures for fault-finding and debugging in new computer chips, fuels the need for an adequate atomic-scale metrology.

Here, members of the PARADIM In-House Team used our Cornell-designed electron microscope pixel array detector (EMPAD-G2) to collect and reconstruct a three-dimensional view inside a modern device using electron ptychography—a technique that holds the world record in microscopy resolution and is available to all users. In collaboration with semiconductor industry partners a special variety of ptychography is used to calculate a three-dimensional reconstruction of the sample that shows atomic-scale details of buried structures along the narrow silicon channel (d), like hafnium oxide intrusions (red arrows) or step edges (green arrow)—all contributing to interface roughness that can impede the performance of the entire electronic device—features that are either inaccessible or easily missed with conventional imaging methods.



a) Overview SEM image of a gate-all-around test structure node (top view, early process development, expected to contain many defects, scale bar: 3 μm). **b)** Cross-section (lamella) along red-dotted line showing 63 gate-all-around columns (3 per stack; scale bar: 0.5 μm). **c)** magnified view, highlighting five columns (scale bar: 50 nm). **d)** common TEM image of a single structure with labels. The hafnium oxide intrusions into the silicon channel are visible (red arrow, scale bar: 5 nm). **e-g)** 3D ptychography reconstruction and slices at two depths show interface roughness, hafnium oxide intrusion (red arrow) and a step edge at the crystalline-silicon/amorphous-silicon oxide interface (green arrow); f,g scale bars: 3 nm.

S. Karapetyan, *et al.* *Nat. Commun.* **17**, 3561 (2026).
Dataset and software codes 10.5281/zenodo.15882443.